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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/577,457	04/27/2006	Takamitsu Yamanaka	AI-409NP	5045
23995	7590	06/24/2009	EXAMINER	
RABIN & Berdo, PC 1101 14TH STREET, NW SUITE 500 WASHINGTON, DC 20005			CHIHAYA, SWAPNEEL	
ART UNIT	PAPER NUMBER			
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/577,457	Applicant(s) YAMANAKA, TAKAMITSU
	Examiner SWAPNEEL CHHAYA	Art Unit 2895

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If no period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED. (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 24 March 2009.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-4 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-4 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) 4-17 are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 27 April 2006 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO-146/08)
 Paper No(s)/Mail Date _____

4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date _____
 5) Notice of Informal Patent Application
 6) Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshihiro (JP 06-268162). In view of Jeng et. al. (U.S. Patent 6136643)

1. Yoshihiro discloses:

A semiconductor device comprising:

a semiconductor substrate (Fig. 1 10 page 2 paragraph 0013)

a first region defined on the semiconductor substrate and having a first device formation region isolated by a device isolation portion formed by filling an insulator in a trench (33) formed in the semiconductor substrate; (Fig. 1 page 2 paragraphs 0013-0016)

a first device (30) provided in the first device formation region (Fig. 1 page 2 paragraph 0014-0015)

a second region (33) defined on the semiconductor substrate separately from the first

region and having a second device formation region (Fig. 1 page 2 paragraph 0014) and

a second device provided in the second device formation region and having a higher breakdown voltage than the first device, the second device having a drift drain structure in which a LOCOS oxide film thicker than a gate insulation film thereof is disposed at an edge of a gate electrode thereof. (Fig. 1-2 page 2 paragraph 0014-0015), please note that the drift drain structure is defined in the specification of the applicant wherein the concentration of the electric field is prevented by locating the thick oxide film at the edge of the gate electrode

Jeng discloses:

Wherein a surface of the device isolation portion and a surface of the semiconductor substrate are both arranged in a common plane (column 2 lines 35-46)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to create the STI that is planar with the substrate surface as taught by Jeng, since Jeng states at column 2 lines 35-46 that such a modification would electrically isolate each device area in and on the substrate.

2.

A semiconductor device as set forth in claim 1,
wherein the second device formation region is a region isolated by a device isolation portion formed by filling an insulator in a trench formed in the semiconductor substrate. (Fig. 1 page 2 paragraphs 0013-0016)

3.

A semiconductor device as set forth in claim 1,

wherein the second device formation region is a region isolated by a LOCOS oxide film.
(Fig. 1-2 page 2 paragraph 0014-0015),

4.

A semiconductor device as set forth in claim 1, wherein the first device has a smaller device size than the second device. (Fig.1)

Response to Arguments

3. Applicant's arguments with respect to claims 1-4 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SWAPNEEL CHHAYA whose telephone number is (571)270-1434. The examiner can normally be reached on Monday- Thursday 9:30-7:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards can be reached on 571-272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SC
/N. Drew Richards/
Supervisory Patent Examiner, Art Unit 2895